Edited by Bill Travis and Anne Watson Swager

Controller supports differential monitor display

William Grill, Riverhead Systems, Littleton, CO

YOU CAN ASSEMBLE A DIFFERENTIAL monitoring display using rail-to-rail analog hardware and a 12C671 eight-pin controller (Microchip Technology, www.microchip.com) (**Figure 1**). The controller, IC_1, reads the scaled analog input reference into its internal ADC at an approximately 3-msec rate. The controller's program provides a dynamic display to the four LEDs based on the deviation from an initially set sensor or monitored value. The "rolling" display moves from end to end at a rate based on the direction and magnitude of the deviation. You can download the accompanying program from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2373.

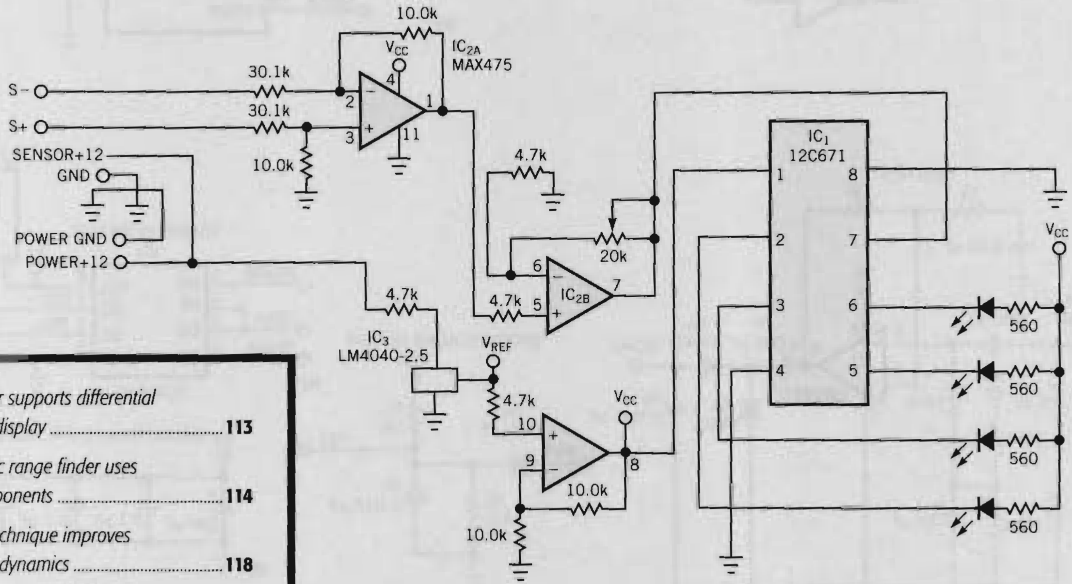
To use the circuit, you apply the reference level and adjust the gain at Pin 7 of IC_{2B} to bring the display to an "all-lite" condition. This adjustment artificially sets the reference to half of the internal ADC's span. The absolute value of the deviation about this reference setting is scaled into eight equal steps above and below this fixed reference to the limits of the converter. For a 5V application, this results in approximately 0.31V indexes ((5/2)/8). The circuit passes the resulting index to a rate table, which sets the display update period. A second index pointer increments each time the display's update period times out. Positive deviations from the reference increment this mask pointer, and negative deviations decrement the pointer. This second pointer then indexes through a mask table, which defines the display's pattern.

The controller uses 127 bytes of code with the eight-step rate table, the relatively small display, and the related 7-byte mask sequence. A stable reference, IC_3, reduces the display's drift over time and temperature.

Although this format is too inflexible to use for all types of monitoring, you could add filtering and span and offset adjustments to provide a more flexible deviation display. You could also implement an expanded display using a 16C710 µC (MicroChip Technology), an external PLD, or one of several 74xx decoders. (DI #2373)

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 395

Figure 1



Controller supports differential monitor display **113**
Ultrasonic range finder uses few components **114**
Simple technique improves transient dynamics **118**
Multiplying DAC makes programmable resistor **120**
Equip switchers with overcurrent protection **122**

The controller's program for this differential monitoring display provides a dynamic display to the four LEDs based on the deviation from an initially set sensor or monitored value.

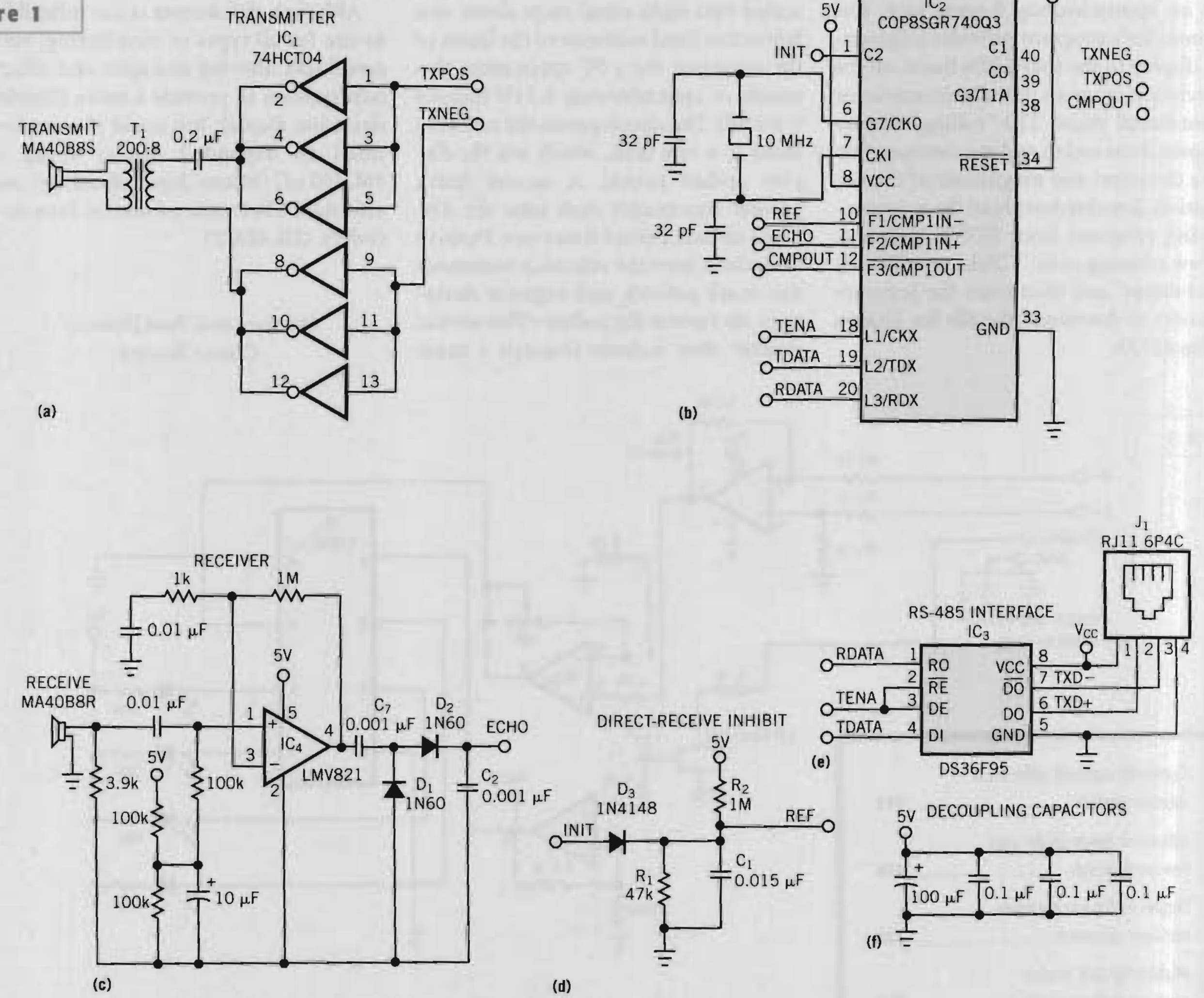
Ultrasonic range finder uses few components

Daniel R Herrington, National Semiconductor, Arlington, TX

An ultrasonic, or sonar, range finder is a common sensor in robotic systems and industrial environments. Even home and automotive uses are possible. A novel sensor design consists of a μC, a few peripheral components, and a pair of ultrasonic transducers (**Figure 1**). The range-finder module consists of a μC, a transmitter, a receiver, a direct-receive inhibit circuit, and an RS-485 interface. The module's usable range is approximately 4 in. to 16 ft with an accuracy of approximately ±2 in. This performance is sufficient for many industrial, automotive, and robotic uses.

Measuring distance with ultrasonic signals requires a transmitting ultrasonic transducer; a medium, such as air or water; a reflecting surface or object; a receiving ultrasonic transducer; and a time-of-flight measurement circuit. The

Figure 1



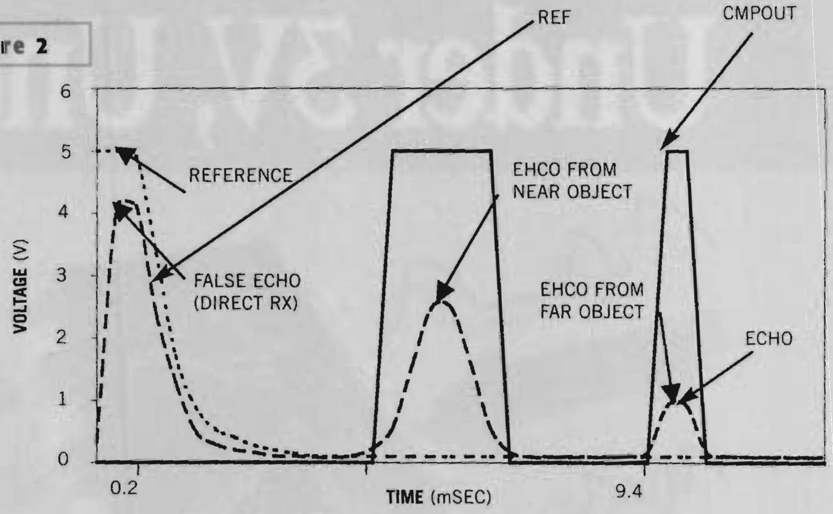
The range-finder module consists of five main subcircuits: a transmitter (a), a μC (b), a receiver (c), a direct-receive inhibit circuit (d), and an RS-485 interface (e), in addition to the requisite decoupling capacitors (f).

speed of sound in air at 20°C is approximately 343m/sec, which translates to about 1 in. per 74 μsec. Doubling the time gives you the round-trip speed, which is 1 in. per 148 μsec. Four aspects of the system limit the maximum measurable distance: the amplitude of the sound wave, the texture of the reflecting surface, the angle of the surface with respect to the incident sound wave, and the sensitivity of the receiving transducer. The receiving transducer's direct reception of the sonar pulse—and not the echo—usually dictates the minimum measurable distance. Although you can use a discrete timer circuit to measure the time of flight, a μC can simplify the hardware design. Using a μC makes it easy to store and serialize the data and then transmit it to a PC or other master controller. The COP8SGR μC from National Semiconductor (www.national.com) includes peripheral blocks, such as timers, analog comparators, and a hardware UART. These peripherals reduce the amount of external hardware or internal software necessary to process the sensory data.

In **Figure 1**, the μC, IC_2, waits for an "address" from a host controller over the RS-485 interface. When it receives the correct slave address, IC_2 begins a 250-μsec pulse of 40 kHz to the ultrasonic transmitter circuit. The μC outputs a high INIT signal to charge C_1. During the transmit pulse, IC_1 drives audio transformer T_1 in a push-pull manner to generate about 40 to 50V p-p across the transducer. In **Figure 1**, the transmit and receive transducers are the matching MA40B8S and MA40B8R (MuRata, www.murata.com), respectively. At the end of the transmit pulse, the μC brings the INIT line low again and C_1 discharges through R_1 to the level that voltage divider $R_1/(R_1+R_2)$ dictates. D_3 keeps the current from flowing back into IC_2's PORTC2 (INIT) pin.

The circuit uses the decaying voltage on the REF signal as a reference for the incoming echo (**Reference 1**). Op amp IC_4 amplifies the echo from the receive transducer. After amplification, D_1 and D_2 rectify the signal to a positive voltage. C_2 smoothes the resulting signal, and the circuit sends this preprocessed echo signal to IC_2's onboard analog comparator.

Figure 2



By comparing the ECHO and REF signals, the range-finder circuit effectively inhibits the large-amplitude receive signal at time t=0.2 msec.

The CMPOUT signal feeds back into IC_2's T1A pin to perform an input-capture operation on the result of the comparison. A positive edge on the T1A pin causes IC_2's Timer 1 to latch the current countdown value in microseconds. Subsequent scaling reduces the 16-bit measurement in microseconds to an 8-bit value that represents distance in inches. The circuit transmits this 8-bit value back over the RS-485 interface, IC_3, to the host controller.

An assembly-code program performs all of the software processing necessary for ultrasonic distance measurement. The program is available for downloading from *EDN*'s web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2371.

Figure 2 shows an example of the three waveforms: REF, ECHO, and CMPOUT. The comparison of the ECHO and REF signals effectively inhibits the large-amplitude signal received directly from the transmitter at time t=0.2 msec. This method allows the minimum measurable distance to be as low as approximately 4 in. This method also eliminates the need for an ADC, as well as the problems associated with defining a threshold value based on some moving average of echo samples.

You can improve the module by adding multiple-echo-detection capability, which allows a single transmitted ultrasonic pulse to recognize two or more objects at different distances (**Figure 2**). You can also incorporate this capability by having the program store the capture value for the first echo, at time t=5 msec, for example, and then re-enable the input-capture countdown and wait for the second capture at time t=9.4 msec, and so on. Another possible improvement is to add servo control to the circuit using one of the internal timers in mode. You can control hobby servos that you commonly find in radio-controlled toys with a 1- to 2-msec-wide positive pulse every 20 msec. In PWM mode, the μC's timers require the loading of only a high width value and a low width value to generate this type of output signal. If you add servo control, you can use the sonar module to measure distance in a given direction. (DI #2371)

REFERENCE

1. Ultrasonic Sensor Application Manual, MuRata Electronics North America Inc, Smyrna, GA, www.murata.com.

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 396

Simple technique improves transient dynamics

Robert Sheehan, Linear Technology Corp, Milpitas, CA

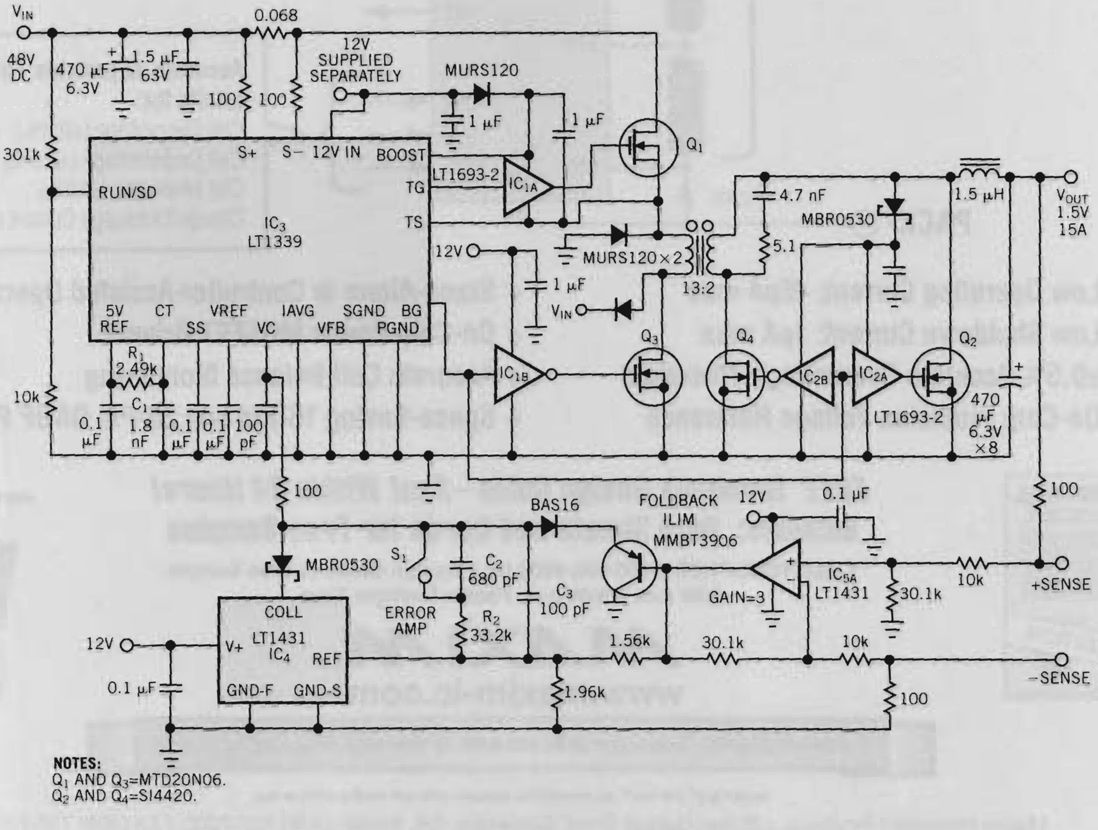
DESIGNING LOW-VOLTAGE, high-current converters with fast dynamic performance places stringent demands on a system designer. However, a simple technique reduces the peak voltage deviation and decreases the response time for a transient load step (**Figure 1**). This circuit converts 48V dc to 1.5V at 15A using a two-transistor forward converter with synchronous rectifiers. Q_1 and Q_3 are primary-side switches. Q_2 and Q_4 are the secondary-side rectifiers. IC_1 and IC_2, a pair of dual MOSFET drivers, provide the gate drive. The circuit derives the power for IC_2 by rectifying the peak secondary voltage. This feature, which allows IC_2 to operate with a 6V supply instead of a 12V supply, reduces gate-drive losses without any significant increase in rectifier conduction losses. IC_3, a high-power, synchronous switching-regulator controller, is at the heart of the PWM control. R_1 and C_1 set the oscillator frequency to just under 200 kHz and limit the maximum duty cycle to 50%.

IC_4, a programmable reference, functions as an error amplifier, overriding IC_3's internal g_m amplifier. This design feature allows for greater control in tailoring the frequency-response characteristics and provides much greater accuracy. You can implement an added feature for output-voltage programming using the summing junction at the REF pin node. Differential amplifier IC_{5A} allows real remote sensing of the output voltage and makes it possible to produce output voltages well below the 2.5V reference of IC_4.

The circuit configures C_2, R_2, and C_3 in a classic Type 2 feedback-amplifier network. The center oscilloscope trace in **Figure 2** shows the response to a 100-nsec load step of 5 to 15A (100A/µsec). The peak-to-peak deviation is 96.8 mV with a settling time of approximately 40 µsec.

Modifying the feedback network can produce significant improvement. Shorting C_2 with S_1 limits the dc gain of the error amplifier, causing the output volt-

Figure 1

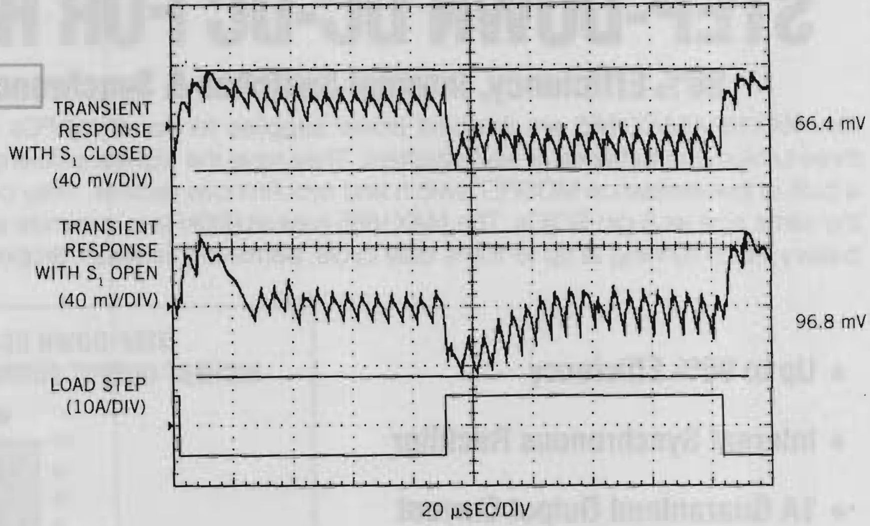


A two-transistor forward converter, Q_1 and Q_3, with synchronous rectifiers Q_2 and Q_4 converts 48V dc to 1.5V at 15A.

age to deviate ±15 mV around its nominal value at half-load. This modification programs the output voltage to move slightly in the direction in which it already wants to go when the load steps. This change also removes the long tail in the settling response because there is no RC charging in the error-amplifier feedback path. The improvement is dramatic, as the top trace in **Figure 2** shows. The peak-to-peak deviation decreases by 30% to 66.4 mV. The full-load-to-light-load settling time decreases to 20 µsec. The light-load-to-full-load settling time is virtually instantaneous. (DI #2370)

To Vote For This Design, Circle No. 397

Figure 2



OUTPUT-VOLTAGE TRANSIENT RESPONSE

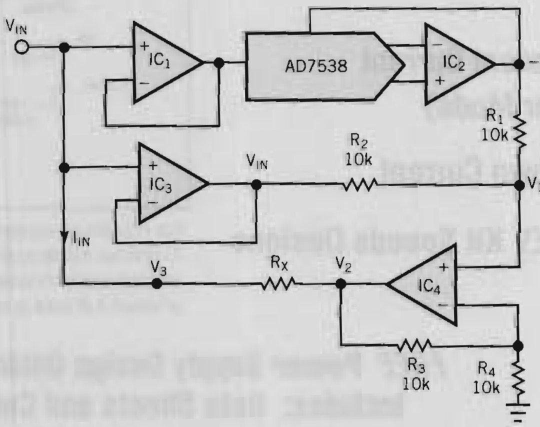
The peak-to-peak deviation with S_1 open is 96.8 mV (center trace). Closing S_1 to short C_2 decreases this deviation to 66.4 mV (top trace.)

Multiplying DAC makes programmable resistor

Albert O'Grady, Analog Devices Inc, Limerick, Ireland

Figure 1 shows a configuration that implements a digitally programmable resistor using a quad op amp and a multiplying DAC. The circuit is equivalent to a voltage-controlled resistor. The simulated resistor has a value that reflects the ratio of a fixed resistor (R_X) and a control voltage. Applications include generating precise resistance values for remotely controlling monostable multivibrators and configuring voltage-controlled loads in simulation circuits. The circuit provides linear control of resistance using the AD7538 14-bit multiplying DAC. You can obtain logarithmic control of the resistance by using an AD7111A logarithmic DAC as the voltage-control element.

Figure 1



A multiplying DAC implements a linear, digitally programmable resistor.

Analysis of the circuit in **Figure 1** reveals the following:

$$V_1 = V_{IN} - \left(\frac{R_2}{R_1+R_2}\right)(V_{IN} + DV_{IN}),$$

where D is input code to the multiplying DAC.

$$V_2 = 1 + V_1\left(\frac{R_3}{R_3+R_4}\right).$$

If R_1=R_2=R_3, then

$$V_2 = V_{IN} - DV_{IN},$$

$$I_{IN} = \frac{V_{IN}-V_2}{R_X} = \frac{DV_{IN}}{R_X}, \text{ and}$$

$$R_{IN} = \frac{V_{IN}}{DV_{IN}/R_X} = \frac{R_X}{D}.$$

The circuit in **Figure 1** operates as a voltage-controlled current source. You can adapt it for use as a basic functional block in the design of a biquad filter. In the adaptation, you modify the circuit to provide a voltage-controlled capacitor rather than a resistor. (DI #2384).

To Vote For This Design, Circle No. 398

Equip switchers with overcurrent protection

Robert N Buono, Buono Consulting, Ringwood, NJ

OVERCURRENT PROTECTION IS usually a necessary design feature of a switch-mode power supply to safeguard both the switcher and the load. Most PWM control ICs have internal overcurrent-protection circuits, and you can typically add auxiliary circuits around the IC to enhance this protection. For example, simple circuits enhance the operation of the common family of UC3842/3/4/5 (Unitrode Corp, www.unitrode.com) PWM-control ICs (**Figure 1**). These circuits allow the switcher to respond to an overcurrent fault condition by latching off if the overcurrent condition persists for more than some defined time interval or by cycling off and then on again at a low duty cycle until the fault clears. When the fault clears, the switcher then resumes normal operation on the next restart cycle. You can add these circuits without affecting other desirable features that the PWM IC may already include, such as soft start and maximum current-limit clamping.

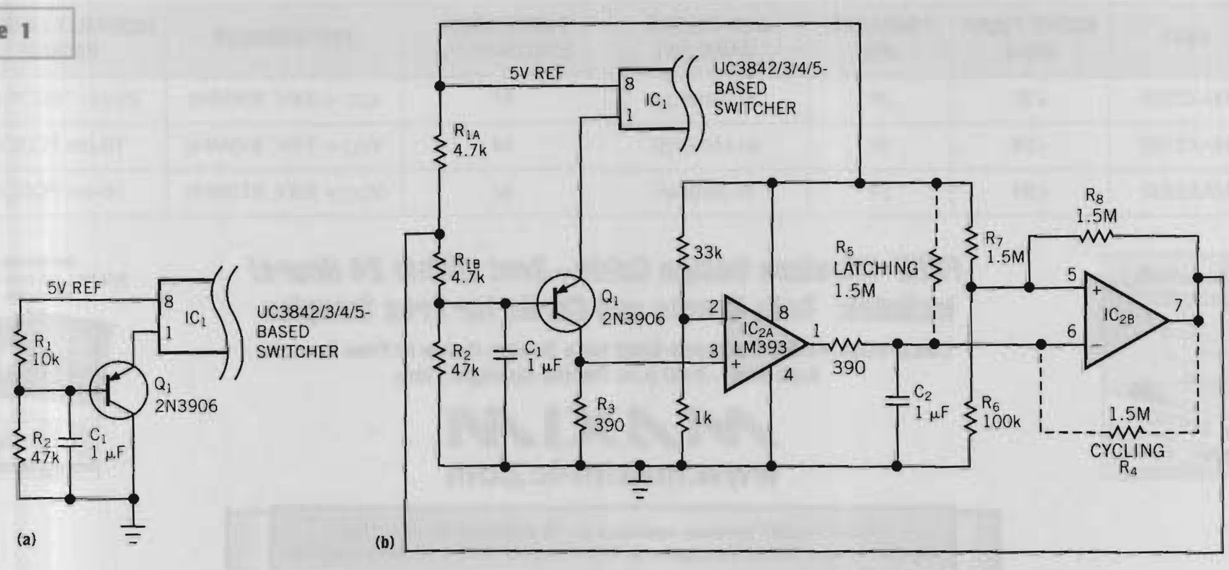
In most switcher designs, operation in current limit imposes the greatest stress on the power devices. Therefore, decreasing the time that the switcher must operate in current-limit mode can enhance the reliability of the switcher. In some cases, decreasing this time may even result in reduced heat-sinking requirements for the power devices. A design that doesn't permit sustained operation in current-limit mode can have a lower average power dissipation than a design that permits a longer time in current-limit mode.

The circuits function solely by manipulating Pin 1 of the PWM IC; the schematics omit all other details of the PWM IC because the remainder of the IC's operation stays the same. In the UC384x family of control ICs, Pin 1 is the output of the internal error amplifier. The voltage at Pin 1 controls and is directly proportional to the peak current level in the main power-switching transistor. Therefore, Pin 1 is a logical place to exert control of the switching current.

The circuit in **Figure 1a** is a commonly used network that adds a slow-start feature as well as maximum current-limit clamping to the PWM- control circuit. The IC's internal error amplifier sources only a limited amount of current, typically 0.8 mA. Therefore, pnp transistor Q_1 easily clamps the voltage at Pin 1 to 0.6V higher than the voltage at its base by diverting the current from Pin 1 through its collector to ground. Thus, the voltage divider of R_1 and R_2 determines the clamping voltage at Pin 1. This voltage sets the maximum current limit of the main power-switching transistor.

A logical conclusion is that adding a capacitor, C_1, from the base of Q_1 to ground will allow a ramp-up characteristic for the clamped voltage at Pin 1 and, therefore, will allow an analogous ramp-up characteristic for the power-switch current. This ramp-up characteristic is usually a desirable feature for initial switcher start-up because it allows the

Figure 1



Manipulating Pin 1 of a UC384x switcher allows you to add more overcurrent protection (a). A dual-comparator circuit allows for cycling or latching off when the switcher is in current-limit mode (b).

switcher's output voltage to ramp up in a controlled manner, reducing output-voltage overshoot. The 5V REF supply in **Figure 1** is a precision voltage reference that IC_1 develops internally. This 5V REF is commonly used to power auxiliary circuits; this output delivers as much as 20 mA. The circuits in **Figure 1** are very low-power, and draw only a small fraction of that available current.

The design in **Figure 1b** adds a low-cost, dual-comparator circuit to the network at Pin 1. R_2 and C_1 remain the same, but this circuit splits R_1 into R_{1A} and R_{1B}. R_3 is an additional component in the collector leg of Q_1. Whenever Q_1 clamps the output of IC_1's Pin 1, a voltage develops across R_3. This voltage indicates the onset of current limiting. R_3 does not interfere with the soft-start and maximum-current-limit clamp performance.

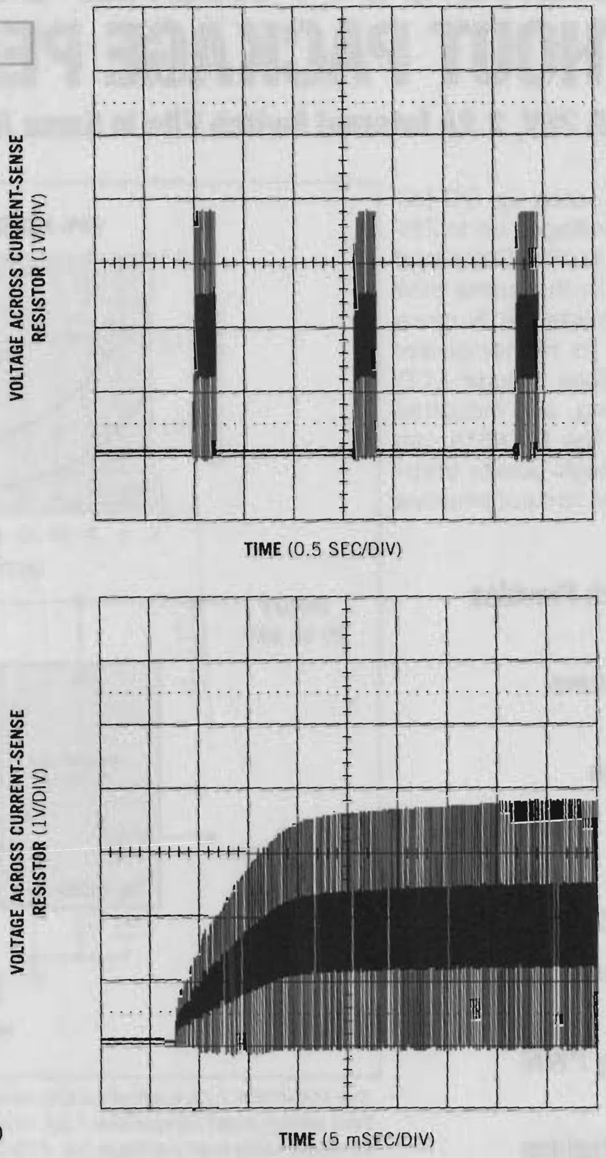
Cycling occurs when you install R_4 and remove R_5. When the switcher is in current-limit mode, a voltage of approximately 400 mV develops across R_3. When the voltage across R_3 exceeds the voltage at IC_{2A}'s Pin 2, which is approximately 150 mV, the output at IC_{2A}'s Pin 1 becomes an open-collector output and allows C_2 to charge through R_4. The time it takes for C_2 to charge from approximately 0V to the threshold established at IC_{2B}'s Pin 5 is the "fault-delay time." During fault-delay time, the switcher remains on and in current-limit mode. IC_{2B} functions as a low-frequency oscillator with low duty cycle. When the voltage on C_2 exceeds the voltage on IC_{2B}'s Pin 5, the open-collector output of IC_{2B} switches low. This low level pulls the base of Q_1 to ground through R_{1B}, and the voltage at Pin 1 of IC_1 clamps to approximately 0.6V. When Pin 1 of IC_1 is less than approximately 1.1V, current through the power-switching transistor is 0A, and the switcher is off.

The resistor ratios of R_6, R_7, and R_8 define the duty cycle of the low-frequency oscillator. For the values shown, the duty cycle is approximately 12%; the switcher is off for 1.4 sec and on for 200 msec. Each time the switcher restarts, it does so with soft start because the output of IC_{2B} fully discharges C_1 through R_{1B}. When the circuit pulls the base of Q_1 low, collector current continues to flow; the circuit maintains the voltage across R_3 even when the switcher is off. IC_{2B} continues to cycle until the overcurrent fault clears. When the fault clears, the circuit reestablishes the nominal output voltage of the switcher, and the voltage at IC_1 Pin 1 drops below the clamp level. The voltage across R_3 drops to 0V and ensures an open-collector output at IC_{2B}'s oscillator output.

Removing R_4 and adding R_5 causes the switcher to latch off and not restart, in response to current limit. You can adjust the ratios of R_6, R_7, and R_8 to optimize the fault-delay time. Increasing the threshold voltage at IC_{2B}'s Pin 5 increases the fault-delay time before latch-off.

Oscilloscope waveforms (**Figure 2**) show the power-switch current cycling on and off when the switcher is in current-limit mode (**Figure 2a**). A time expansion of the ramp-characteristic of the power-switch current for each restart event shows that each restart benefits from the soft-start characteristic (**Figure 2b**). These waveforms are the result of measuring the voltage across a current-sensing resistor; the waveforms represent the current through the main power-switching transistor switching at 50 kHz.(DI #2369)

Figure 2



The power-switch current cycles on and off when the switcher is in current limit (a). Each restart benefits from soft start (b).

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 399